Amendments to the Claims

1. (*Currently Amended*) Semiconductor device comprising

a vertical split gate non-volatile memory cell, for storing at least one bit, on a semiconductor substrate ~~(1)~~, comprising on said substrate

_____~~(1)~~ a trench ~~(4)~~,

_____a first active area ~~(6)~~,

_____a second active area ~~(15)~~,

_____a channel region ~~(er)~~ extending substantially along a side wall of said trench ~~(4)~~,

_____said trench ~~(4)~~ having a length in a first direction ~~(A-A')~~ and a width in a second direction ~~(B-B')~~, said first direction being perpendicular to said second direction,

_____said trench ~~(4)~~ being covered on said side walls by a tunnel oxide ~~(5)~~ and comprising at least one gate stack ~~(S1, S2)~~,

_____said gate stack ~~(S1, S2)~~ consisting of a floating gate ~~(7")~~ and a control gate ~~(13)~~,

_____said floating gate ~~(7")~~ being separated from said control gate ~~(13)~~ by a dielectric ~~(12)~~, characterised in that said control gate ~~(13)~~ extends to the bottom part of said trench ~~(4)~~,

_____a first floating gate ~~(7")~~ is located at a left side wall of said trench ~~(4)~~ to form a first gate stack ~~(S1)~~ with said control gate ~~(13)~~, and a second floating gate ~~(7")~~ is located at a right side wall of said trench ~~(4)~~ to form a second gate stack ~~(S2)~~ with said control gate ~~(13)~~.

2. (*Currently Amended*) Semiconductor device according to claim 1, characterised in that said dielectric ~~(12)~~ extends along an upper exposed part ~~(U)~~ of said side wall of said trench ~~(4)~~; and said control gate ~~(13)~~ extends along said dielectric ~~(12)~~ covering said upper exposed part ~~(U)~~ of said side wall of said trench ~~(4)~~.

3. (*Currently Amended*) Semiconductor device ~~according to claim 1 or 2,~~ according to claim 1, characterised in that said first floating gate ~~(7")~~ and said second floating gate ~~(7")~~ are interconnected by an interconnecting poly-Si portion.

4. (*Currently Amended*) Semiconductor device ~~according to claim 1 or 2,~~ according to claim 1, characterised in that said first floating gate ~~(7")~~ and said second floating gate ~~(7")~~ are isolated from each other.

5. (Currently Amended) Method for fabrication of a semiconductor device comprising a vertical split gate non-volatile memory cell, ~~according to claim 1 or 2 or 3 or 4,~~ according to claim 1, characterised in that said method ~~comprises the following steps:~~ comprises:
~~(PS-VIII) :~~ depositing poly-Si ~~(7)~~ in said trench ~~(4)~~, said poly-Si ~~(7)~~ having a planarised top surface;
~~(PS-X - PS-XIII) :~~ forming isolation slits ~~(4')~~ by a silicon dioxide ~~(9)~~ in said trench ~~(4)~~ for isolating said memory cell in said second direction by using a slit mask ~~(M2)~~;
~~(PS-XIV) :~~ back-etching of said poly-Si ~~(7)~~;
~~(PS-XV):~~ back-etching of said silicon dioxide ~~(9)~~;
~~(PS-XVI) :~~ forming first spacers ~~(10)~~ extending in said second direction on said planarised top surface of said poly-Si and second spacers ~~(11)~~ extending in said first direction on said silicon dioxide ~~(9)~~;
~~(PS-XVII, PS-XVIII) :~~ etching of said poly-Si by a reactive ion etching process using said first spacers ~~(10)~~ and said second spacers ~~(11)~~ as a mask to form an etched recessed poly-Si portion serving as a floating gate ~~(7")~~, and a lower exposed part ~~(S)~~ of said trench ~~(4)~~;
~~(PS-XIX) :~~ forming said dielectric ~~(12)~~ on said floating gate ~~(7")~~ and said lower exposed part ~~(S)~~ of said trench ~~(4)~~;
~~(PS-XX) :~~ depositing a second poly-Si layer over said dielectric ~~(12)~~;
~~(PS-XXI) :~~ planarising said second poly-Si used as said control gate ~~(13)~~ extending from the top of said trench ~~(4)~~ to the bottom of said trench ~~(4)~~ covers said dielectric ~~(12)~~.

6. (*Currently Amended*) Method for fabrication of a semiconductor device according to claim 5, characterised in that said method further ~~comprises in:~~ comprises:

~~(PS-XVII, PS-XVIII) :~~ _____the formation of an upper exposed part (U) of said side wall of said trench (4);

~~(PS-XIX) :~~___ the formation of said dielectric ~~(12)~~ on said upper exposed part ~~(U)~~ of said side wall of said trench ~~(4)~~.

7. (*Currently Amended*) Method for fabrication of a semiconductor device according to claim 5 or 6, according to claim 5, characterised in that said method ~~comprises as further steps:~~ further comprises:

~~(PS-XXIV) :~~_forming further spacers ~~(21, 22)~~ adjacent to said control gate ~~(13)~~ on said top surface;

~~(PS-XXV) :~~__implantation of said second active area ~~(15)~~;

~~(PS-XXVI) :~~_silicidation of said control gate ~~(13)~~ and said drain ~~(15)~~;

~~(PS-XXVII) :~~_creation of conductive connections ~~(17; 17')~~ to said control gate ~~(13)~~.

8. (*Currently Amended*) Method for fabrication of a semiconductor device according to claim 7, characterised in that

_____said poly-Si ~~(7)~~ has a silicon surface level,

_____said silicon dioxide ~~(9)~~ has an oxide surface level, and

_____said silicon nitride ~~(2')~~ has a nitride surface level, said silicon surface level being arranged below said nitride surface level, said oxide surface level being arranged below said silicon surface level and above said channel region ~~(er)~~ to allow formation of said second spacers ~~(11)~~ on said silicon oxide ~~(9)~~ without formation on said poly-Si ~~(7)~~.

9. (*Currently Amended*) Method for fabrication of a semiconductor device according to claim 7, characterised in that

said poly-Si ~~(7)~~ has a silicon surface level,

said silicon dioxide ~~(9)~~ has an oxide surface level, and

said silicon nitride ~~(2')~~ has a nitride surface level, said silicon surface level being arranged substantially equal to said nitride surface level, said oxide surface level being

arranged substantially equal to said silicon surface level and said channel region ~~(cr)~~ to allow simultaneous formation of said first spacers ~~(10)~~ on said poly-Si ~~(7)~~ and said second spacers ~~(11)~~ on said silicon oxide ~~(9)~~, said first and second spacers ~~(10, 11)~~ having substantially equal thickness and height.

10. (*Currently Amended)* Method for fabrication of a semiconductor device ~~according to claim 3 or 4,~~ according to claim 3, characterised in that ~~said method comprises the following steps:~~ said method comprises:

~~(PS-VIII) :~~ depositing poly-Si ~~(7)~~ in said trench ~~(4)~~, said poly-Si ~~(7)~~ having a top surface;

~~(PS-X - PS-XIII) :~~ forming isolation slits ~~(4')~~ by a silicon dioxide ~~(9)~~ in said trench ~~(4)~~ for isolating said memory cell in said second direction by using a slit mask ~~(M2)~~;

~~(PS-XVI) :~~ forming first spacers ~~(10)~~ extending in said second direction and second spacers ~~(11)~~ extending in said first direction on said top surface of said poly-Si;

~~(PS-XVII, PS-XVIII) :~~ etching of said poly-Si by a reactive ion etching process using said first spacers ~~(10)~~ and second spacers ~~(11)~~ as a mask to form an etched recessed poly-Si portion serving as a floating gate ~~(7")~~, and a lower exposed part ~~(S)~~ of said trench ~~(4)~~;

~~(PS-XIX) :~~ forming said dielectric ~~(12)~~ on said floating gate ~~(7")~~ and said lower exposed part ~~(S)~~ of said trench ~~(4)~~;

~~(PS-XX) :~~ depositing a second poly-Si layer over said dielectric ~~(12)~~;

~~(PS-XXI) :~~ planarising said second poly-Si used as said control gate ~~(13)~~ extending from the top of said trench ~~(4)~~ to the bottom of said trench ~~(4)~~ covers said dielectric ~~(12)~~;

~~(PS-XXIIa) :~~ a second patterning by means of said slit mask ~~(M2)~~;

~~(PS-XXIIb) :~~ reactive ion etching of poly-Si over said silicon dioxide ~~(9)~~;

~~(PS-XXIIc) :~~ depositing of a further silicon dioxide in blanket mode and planarising said further silicon dioxide.

11. (*Currently Amended*) Method for fabrication of a semiconductor device ~~according to claim 3 or 4,~~ according claim 3, characterised in that said method ~~comprises the following steps:~~ comprises:

~~(PS-VIII) :~~ depositing poly-Si ~~(7)~~ in said trench ~~(4)~~, said poly-Si ~~(7)~~ having a top surface;

~~(PS-X - PS-XIII) :~~ forming isolation slits ~~(4')~~ by a silicon dioxide ~~(9)~~ in said trench ~~(4)~~

for isolating said memory cell in said second direction by using a slit mask ~~(M2)~~;

~~(PS-XIVa) :~~ a second application of said slit mask ~~(M2)~~;

~~(PS-XIV) :~~ back-etching of said poly-Si ~~(7)~~;

~~(PS-XV) :~~ back-etching of said silicon dioxide ~~(9)~~;

~~(PS-XVI) :~~ forming said first spacers ~~(10)~~ extending in said first direction on said top surface of said poly-Si;

~~(PS-XVII, PS-XVIII) :~~ etching of said poly-Si by a reactive ion etching process using said first spacers ~~(10)~~ and said second spacers ~~(11)~~ as a mask to form an etched recessed poly-Si portion serving as a floating gate ~~(7")~~, and a lower exposed part ~~(S)~~ of said trench ~~(4)~~;

~~(PS-XIX) :~~ forming said dielectric ~~(12)~~ on said floating gate ~~(7")~~ and said lower exposed part ~~(S)~~ of said trench ~~(4)~~;

~~(PS-XX) :~~ depositing a second poly-Si layer over said dielectric ~~(12)~~;

~~(PS-XXI) :~~ planarising said second poly-Si used as said control gate ~~(13)~~ extending from the top of said trench ~~(4)~~ to the bottom of said trench ~~(4)~~ covers said dielectric ~~(12)~~.

12. (*Currently Amended*) Method for fabrication of a semiconductor device ~~according to any of the preceding claims 5-12,~~ according to claim 5, characterised in that said method further comprises :

~~(PS-Ib) :~~ as an initial process the implantation of said first active area ~~(6)~~ using an implantation mask substantially corresponding to said trench mask ~~(M1)~~.

13. (*Currently Amended*) Method for fabrication of a semiconductor device ~~according to any of the preceding claims 5-13,~~ according to claim 5, characterised in that said creation of conductive connections relates to the creation of metal lines ~~(17)~~.

14. (*Currently Amended*) Method for fabrication of a semiconductor device ~~according to any of the preceding claims 5-13,~~ according to claim 5, characterised in that said creation of conductive connections relates to the creation of silicided control gate lines ~~(17')~~ and silicided drain lines ~~(15'; 15")~~.

15. (*Currently Amended*) Array of memory cells comprising at least one vertical split gate non-volatile memory cell ~~according to any of the preceding claims 1, 2, 3, or 4.~~ according to claim 1.

16. (*New*) Array of memory cells comprising at least one vertical split gate non-volatile memory cell according to claim 2.

17. (*New*) Array of memory cells comprising at least one vertical split gate non-volatile memory cell according to claim 3.

18. (*New*) Array of memory cells comprising at least one vertical split gate non-volatile memory cell according to claim 4.